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EXAMINER	
SHAPIRO, LEONID	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/747,194	Applicant(s) YOKOYAMA, RYOICHI	
	Examiner Leonid Shapiro	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 5-6, 40, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (US Patent No. 5,945,972) in view of Sato et al. (US Patent No. 5,712,652).

As to claim 1, Okumura et al. teaches a display apparatus with: a plurality of gate lines provided in one direction of a substrate (See Fig. 2B, items La1, La2..., in description See Col. 12, Lines 52-53); a plurality of drain lines provided in a direction intersecting with gate lines (See Fig. 2B, items Lb1, Lb2..., in description See Col. 12, Lines 52-53); a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of plurality of gate lines, and which is supplied with an image signal from corresponding one of plurality of drain lines; wherein each of plurality of display pixels with: a display element (See Fig. 2B, 3, item CEL, in description See Col. 13, Lines 16-24); a storing circuit for storing a digital image signal from corresponding one of plurality of drain lines in response to a scan signal from corresponding one of gate lines (See Fig. 2B, 3, items PDC,121a,121b,123,124, in description See Col. 13, Lines 39-49).

Okumura et al. does not show a signal selector which is operated based on data stored at storing circuit for selecting an output signal from among two or more display signals and for supplying selected signal to display element.

Sato teaches a structure wherein, in each pixel, transfer gates correspondent to a signal selector and connected to AC drive signal and reset signal (constant voltage identical to the voltage on the opposing electrode) and, based on data stored (two inverters), one of transfer gates is operated so that an AC drive signal of the constant voltage can be output to the liquid crystal (See Fig. 1, items, 8-11, 100, in description See Col. 9, Lines 36-67).

It would have been obvious to one ordinary skill in the art at time of the invention to implement a signal selector with AC drive and reset signals as shown by Sato et al. and replace the reset signal with DC voltage in the Okumura et al. apparatus in order to improve the image quality (See Col. 2, Lines 30-33 in Okumura et al. reference) and reduce power consumption (See Col. 2, Lines63-65 in Sato et al. reference).

As to claim 40, Okumura et al. teaches a display apparatus with : a plurality of gate lines provided in one direction of a substrate (See Fig. 2B, items La1, La2…, in description See Col. 12, Lines 52-53); a plurality of drain lines provided in a direction intersecting with gate lines (See Fig. 2B, items Lb1, Lb2…, in description See Col. 12, Lines 52-53); a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of plurality of gate lines, and which is supplied with an image signal from corresponding one of plurality of drain lines; wherein each of plurality of display pixels with: a display element (See Fig. 2B, 3, item CEL, in description See Col. 13, Lines 16-24); a storing circuit for storing one-bit digital image signal from corresponding one of plurality of drain lines in response to a scan signal from corresponding one of gate lines (See Fig. 2B, 3, items PDC,121a,121b,123,124, in description See Col. 13, Lines 39-49).

Okumura et al. does not show a signal selector which is operated based on the digital signal stored at storing circuit for selecting an output signal from among two or more display signals and for supplying selected signal to display element and a switching element which is operated based on a scan signal from corresponding one of plurality of gate lines for capturing a one-bit digital image signal corresponding one of drain lines.

Sato teaches a structure wherein, in each pixel, transfer gates correspondent to a signal selector and connected to AC drive signal and reset signal (constant voltage identical to the voltage on the opposing electrode) and, based on data stored (two inverters), one of transfer gates is operated so that an AC drive signal of the constant voltage can be output to the liquid crystal (See Fig. 1, items, 8-11, 100, in description See Col. 9, Lines 36-67) and a switching element which is operated based on a scan signal from corresponding one of plurality of gate lines for capturing a one-bit digital image signal corresponding one of drain lines (See Fig. 1, items 6-7, in description See Col. 9, Lines 43-46).

It would have been obvious to one ordinary skill in the art at time of the invention to implement a signal selector with AC drive and reset signals, and capturing a one-bit digital image signal by as shown by Sato et al. and replace the reset signal with DC voltage in the Okumura et al. apparatus in order to improve the image quality (See Col. 2, Lines 30-33 in Okumura et al. reference) and reduce power consumption (See Col. 2, Lines63-65 in Sato et al. reference).

As to claim 42, Okumura et al. teaches a display apparatus with: a plurality of gate lines provided in one direction of a substrate (See Fig. 2B, items La1, La2…, in description See Col. 12, Lines 52-53); a plurality of drain lines provided in a direction intersecting with gate lines

(See Fig. 2B, items Lb1, Lb2..., in description See Col. 12, Lines 52-53); a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of plurality of gate lines, and which is supplied with an image signal from corresponding one of plurality of drain lines; wherein each of plurality of display pixels with: a display element (See Fig. 2B, 3, item CEL, in description See Col. 13, Lines 16-24); a storing circuit for storing a digital image signal having a size of two or more bits supplied from corresponding one of plurality of drain lines (two or more memories with at least one bit) (See Fig. 2B, 3, 5, items PDC,121a,121b, 121m, 123,124, in description See Col. 13, Lines 30-49, Col. 12, Lines 55-60 and Col. 16, Lines 51-53).

Okumura et al. does not show a signal selector which is operated based on data stored at storing circuit for selecting an output signal from among two or more display signals and for supplying selected signal to display element.

Sato teaches a structure wherein, in each pixel, transfer gates correspondent to a signal selector and connected to AC drive signal and reset signal (constant voltage identical to the voltage on the opposing electrode) and, based on data stored (two inverters), one of transfer gates is operated so that an AC drive signal of the constant voltage can be output to the liquid crystal (See Fig. 1, items, 8-11, 100, in description See Col. 9, Lines 36-67).

It would have been obvious to one ordinary skill in the art at time of the invention to implement a signal selector with AC drive and reset signals as shown by Sato et al. and replace the reset signal with DC voltage in the Okumura et al. apparatus in order to improve the image quality (See Col. 2, Lines 30-33 in Okumura et al. reference) and reduce power consumption (See Col. 2, Lines63-65 in Sato et al. reference).

As to claim 2, Okumura et al. teaches a display apparatus wherein storing circuit has a predetermined number of storing elements, number corresponding to the number of bits in digital image signal and signal selector selects a signal to be supplied to display element from among predetermined number of signals, number corresponding to the number of bits in digital image signal (See Fig. 27, item 531, in description See Col. 27, Lines 5-14).

As to claim 5, Okumura et al. teaches a display apparatus, capable of displaying a still image (See Col. 12, Lines 19-34).

As to claim 6, Okumura et al. teaches a display apparatus wherein, after still image is written to each of plurality of display pixels as a digital image signal, operation of driving circuits for driving plurality of display pixels are stopped until a new digital image signal is written to the same display pixels (See in description See Col.12, Lines 12-15).

As to claim 3, Okumura et al. does not teach to use one or more invertors to store digital image signals.

Sato et al. teaches how to use to use one or more invertors to store digital image signals See Fig. 1, items 4-5, in description See Col. 9, Lines 43-46).

It would have been obvious to one ordinary skill in the art at time of the invention to use Sato et al. approach in the Okumura et al. apparatus in order to improve the storage capability and the image quality.

2. Claims 9-17, 20-26, 28-32, 34-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al in view of Yutaka et al. (EP 586155) and Sato et al.

As to claims 9, 20, 22, 28, 34, Okumura teaches a display apparatus with: a plurality of gate lines provided in one direction of a substrate (See Fig. 2B, items La1, La2..., in description See Col. 12, Lines 52-53); a plurality of drain lines provided in a direction intersecting with gate lines (See Fig. 2B, items Lb1, Lb2..., in description See Col. 12, Lines 52-53); a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of plurality of gate lines, and which is supplied with an image signal from corresponding one of plurality of drain lines; wherein each of plurality of display pixels with: a display element (See Fig. 2B, 3, item CEL, in description See Col. 13, Lines 16-24); a first display circuit having a storing circuit, for storing a digital image signal from corresponding one of plurality of drain lines in response to a scan signal from corresponding one of gate lines (See Fig. 2B, 3, items Lai, Lbj, in description See Col. 13, Lines 39-49).

Okumura et al. teaches the display signal may be stored in the first memory circuit in the either digital or analog form (See Fig. 27, items 532, 535, in description See Col. 27, lines 10-14 and Lines 51-55).

Okumura et al. does not show a second display circuit having a storage capacitor for storing an analog image signal from corresponding one of drain lines in response to a scan signal from corresponding one of gate lines, wherein the signal stored in storage capacitor is supplied to display element.

Yutaka et al. teaches how to use capacitor to store analog image data. (See Fig. 10, item Ch, in description See Example 6). It would have been obvious to one ordinary skill in the art at time of the invention to replace one of memory circuit in the Okumura et al. apparatus by the

holding capacitor as shown by Yutaka et al. in order to improve the storage capability and the image quality.

Okumura et al. and Yutaka et al. do not show a signal selector which is operated based on data stored at storing circuit for selecting an output signal from among two or more display signals and for supplying selected signal to display element.

Sato teaches a structure wherein, in each pixel, transfer gates correspondent to a signal selector and connected to AC drive signal and reset signal (constant voltage identical to the voltage on the opposing electrode) and, based on data stored (two inverters), one of transfer gates is operated so that an AC drive signal of the constant voltage can be output to the liquid crystal (See Fig. 1, items, 8-11, 100, in description See Col. 9, Lines 36-67).

It would have been obvious to one ordinary skill in the art at time of the invention to implement a signal selector with AC drive and reset signals as shown by Sato et al. and replace the reset signal with DC voltage in the Okumura et al. and Yutaka et al. apparatus in order to improve the image quality (See Col. 2, Lines 30-33 in Okumura et al. reference) and reduce power consumption (See Col. 2, Lines63-65 in Sato et al. reference).

As to claims 24, 30, 36, Okumura et al. and Yutaka et al. do not show storing circuit, which stores digital image signal using a one or two invertors.

Sato et al. teaches how to use one or more inverters to store a digital image signal (See Fig. 1, items 4, 5, in description See Col. 9, Lines 43-46). It would have been obvious to one ordinary skill in the art at time of the invention to one or more invertors as shown by Sato et al. in the Okumura et al. and Yutaka et al display apparatus in order to improve the storage capability and the image quality.

As to claims 10, Okumura et al. teaches a display circuit selector for selectively supplying an image signal from corresponding one of drain lines in Okumura et al. and Yutaka et al. apparatus (See Fig. 2B, 3, items 125, CEL, in description See Col. 13, Lines 60-67 and Col.14, Lines 1-6, See Fig. 8, 9, items 230a, 230b, 261, 274, 276, in description See Col. 18, Lines 18-21 and 33-36).

As to claims 11, Okumura et al. teaches two memories approach with corresponding one of drain lines is constructed from a line for digital image signals (Memory 1) and a line for analog image signals (Memory 2) and first display circuit is connected for line for analog and digital signals and rewrite control line (See Fig. 2A, 2B, 3, items Lcj, Lbj, Sb, Sc, 124, 123, 121a, 121b, in description See 12, Lines 55-67 and Col. 13, Lines 39-46).

As to claims 12, Okumura et al. teaches a data selector for selectively supplying an output signal from first or second display circuit (Memory 1 and 2) to display element (See Fig. 3, items 121a, 121b, 125, Ss, CEL, in description See Col.13, Lines 59-67).

As to claim 13, Okumura et al. teaches a display apparatus wherein storing circuit has a predetermined number of storing elements, number corresponding to the number of bits in digital image signal and signal selector selects a signal to be supplied to display element from among predetermined number of signals, number corresponding to the number of bits in digital image signal (See Fig. 27, item 531, in description See Col. 27, Lines 5-15).

As to claim 14, Okumura et al. and Yutaka et al. do not show storing circuit stores digital image signal using one or more inverters.

Sato et al. teaches how to use one or more inverters to store a digital image signal (See Fig. 1, items 4, 5, in description See Col. 9, Lines 43-46). It would have been obvious to one

ordinary skill in the art at time of the invention to replace one of memory circuit in the Okumura et al. and Yutaka et al. apparatus by the memory with one or more inverters as shown by Sato et al. in order to improve the storage capability and the image quality.

As to claim 16, Okumura et al. teaches a display apparatus, capable of displaying a still image (See Col. 12, Lines 19-34).

As to claim 17, Okumura et al. teaches a display apparatus wherein, after still image is written to each of plurality of display pixels as a digital image signal, operation of driving circuits for driving plurality of display pixels are stopped until a new digital image signal is written to the same display pixels (See in description See Col.12, Lines 12-15).

As to claims 21, Okumura et al. teaches a display circuit selector for selectively supplying an image signal from corresponding one of drain lines in Okumura et al. and Yutaka et al. apparatus and display circuit selector is switched in response to a switching signal, which is common to a plurality of pixels (See Fig. 2B, 3, items 125, CEL, in description See Col. 13, Lines 60-67 and Col.14, Lines 1-6, See Fig. 8, 9, items 230a, 230b, 261, 274, 276, in description See Col. 18, Lines 18-21 and 33-36).

As to claims 23, 29, 35, Okumura et al. teaches a display apparatus wherein storing circuit has a predetermined number of storing elements, number corresponding to the number of bits in digital image signal and signal selector selects a signal to be supplied to display element from among predetermined number of signals, number corresponding to the number of bits in digital image signal (See Fig. 27, item 531, in description See Col. 27, Lines 5-14).

As to claims 25,31,37, Okumura et al. teaches a display apparatus, capable of displaying a still image (See Col. 12, Lines 19-34).

As to claims 26,32,38 Okumura et al. teaches a display apparatus wherein, after still image is written to each of plurality of display pixels as a digital image signal, operation of driving circuits for driving plurality of display pixels are stopped until a new digital image signal is written to the same display pixels (See in description See Col.12, Lines 12-15).

3. Claims 7-8,18-19,27,33,39 rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al, Yutaka et al. and Sato et al. as aforementioned in claims 1, 9, 22, 28, 34 in view of Hamada (EP 4144780).

Okumura et al, Yutaka et al. and Sato et al. do not show a liquid crystal capacitor and a pair of electrodes for driving liquid crystal capacitor with individual display electrode for each display pixel and a facing electrode provided and at least one of the signals is an alternating current voltage signal oscillates around the voltage of facing electrode.

Hamada teaches how a reversed-phase a. c. voltage is applied to electrode b (See Fig. 4, items a, b, Vc and Vc', in description See Col.10, Lines 9-15). It would have been obvious to one ordinary skill in the art at time of the invention to use alternating current as shown by Hamada and simple multiplexer in the Okumura et al, Yutaka et al. and Sato et al. apparatus in order to display of clear, non-flickering constant image on the screen (See Abstract in the Hamada reference).

4. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al in view of Sato et al. and Schleupen et al. (US Patent N0. 5,517,543)

Okumura et al. teaches a display apparatus with: a plurality of gate lines provided in one direction of a substrate (See Fig. 2B, items La1, La2..., in description See Col. 12, Lines 52-53); a plurality of drain lines provided in a direction intersecting with gate lines (See Fig. 2B, items Lb1, Lb2..., in description See Col. 12, Lines 52-53); a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of plurality of gate lines, and which is supplied with an image signal from corresponding one of plurality of drain lines; wherein each of plurality of display pixels with: a display element (See Fig. 2B, 3, item CEL, in description See Col. 13, Lines 16-24); a storing circuit for storing a digital image signal from corresponding one of plurality of drain lines in response to a scan signal from corresponding one of gate lines (See Fig. 2B, 3, items PDC,121a,121b,123,124, in description See Col. 13, Lines 39-49).

Okumura et al. does not show a signal selector which is operated based on data stored at storing circuit for selecting an output signal from among two or more display signals and for supplying selected signal to display element.

Sato teaches a structure wherein, in each pixel, transfer gates correspondent to a signal selector and connected to AC drive signal and reset signal (constant voltage identical to the voltage on the opposing electrode) and, based on data stored (two inverters), one of transfer gates is operated so that an AC drive signal of the constant voltage can be output to the liquid crystal (See Fig. 1, items, 8-11, 100, in description See Col. 9, Lines 36-67).

It would have been obvious to one ordinary skill in the art at time of the invention to implement a signal selector with AC drive and reset signals as shown by Sato et al. and replace the reset signal with DC voltage in the Okumura et al. apparatus in order to improve the image

quality (See Col. 2, Lines 30-33 in Okumura et al. reference) and reduce power consumption (See Col. 2, Lines63-65 in Sato et al. reference).

Okumura et al. and Sato et al. do not show a storage circuit stores digital image signal using one or more inverters and a capacitor.

Schleupen et al. teaches to use capacitor and buffer amplifier to store image data. (See Fig. 1, items Tn1, Tn2 and Cn1, in description See Col. 4, Lines33-46).

It would have been obvious to one ordinary skill in the art at time of the invention to replace one of memory circuit in the Okumura et al. and Sato et al. apparatus by the holding capacitor and buffer amplifier as shown by Schleupen et al. to store digital image in order to order to improve the image quality (See Col. 2, Lines 30-33 in Okumura et al. reference) and reduce power consumption (See Col. 2, Lines 63-65 in Sato et al. reference).

5. Claim15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al., Yutaka et al. and Sato et al. as applied to claim 9 above, and further in view of Schleupen et al..

Okumura et al., Yutaka et al. and Sato et al. do not show storing circuit stores digital image signal using one or inverters and a capacitor.

Schleupen et al. teaches to use capacitor and buffer amplifier to store image data. (See Fig. 1, items Tn1, Tn2 and Cn1, in description See Col. 4, Lines33-46).

It would have been obvious to one ordinary skill in the art at time of the invention to replace one of memory circuit in Okumura et al., Yutaka et al. and Sato et al. apparatus by the holding capacitor and buffer amplifier as shown by Schleupen et al. to store digital image in

order to order to improve the image quality (See Col. 2, Lines 30-33 in Okumura et al. reference) and reduce power consumption (See Col. 2, Lines 63-65 in Sato et al. reference).

Response to Amendment

6. Applicant's arguments with respect to claims 1-3, 5-42 have been considered but are moot in view of the new ground(s) of rejection.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

ls

VIJAY SHANKAR
PRIMARY EXAMINER